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Search History

DATE: Monday, April 25, 2005 Printable Copy Create Case

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L8: Entry 2 of 5 File: USPT Jul 17, 2001

DOCUMENT-IDENTIFIER: US 6263471 B1
TITLE: Method and apparatus for decoding an error correction code

Brief Summary Text (49):
In accordance with this invention there is further provided an error correction circuit for correcting bit errors in a received codeword encoded by an error correction code over GF(2.sup.m), the circuit comprising: means for generating a syndrome polynomial S(x) by computing power sums of symbols of the received codeword; means for solving the key equation .OMEGA.(x)=.LAMBDA.(x)S(x) mod x.sup.2t to generate an error location polynomial .LAMBDA.(x) representing error locations of the errors in the codeword and an error evaluation polynomial .OMEGA.(x) used to determine error values of the errors; means for determining roots of the error location polynomial .LAMBDA.(x), each of the roots indicating an error location; means for determining error values from the roots; and means for generating a corrected codeword from the error locations, the error values and the received codeword, wherein the means for solving the key equation comprises a one-bit quotient bus for bit-serially transmitting m quotient digits of an m-bit quotient value and a plurality of processing units each bit-serially receiving the quotient digits from the bus and each including: (i) a first m-bit register; (ii) an m-by-one multiplier for multiplying contents of the first register by one of the quotient digits received from the bus to produce an m-bit parallel multiplication result; (iii) a second m-bit register; and (iv) an adder for adding the m-bit multiplication result with contents of the second register to provide an m-bit addition result for replacing the contents of the second register, wherein the m-by-one multiplier comprises m AND gates, the adder comprises m exclusive OR gates, and the second register and the adder are configured to provide an accumulator for accumulating the m-bit multiplication result of the m-by-one multiplier. The apparatus may further comprise an inversion means for generating an m-bit output in response to an m-bit value received from one of the processing units; and a quotient means for generating the m-bit quotient value by multiplying the m-bit output of the inversion means by an m-bit value received from one of the processing units and for transmitting the m-bit quotient value bit-serially on the bus. The first m-bit register forms a linear feedback shift register which multiplies contents of the first register by .alpha. and stores the multiplication result back to the first register, where .alpha. is a non-zero element of GF(2.sup.m).